ABSTRACT OF THE DISCLOSURE

An STI structure and fabricating method thereof are disclosed. The STI fabricating method comprises forming a pad oxide layer and a first nitride layer on a substrate. A trench is formed by etching the first nitride layer, the pad oxide layer and the substrate. An oxide and a second nitride layer are deposited on the surface of the substrate including the trench. A spacer is formed on the lateral walls of the trench by etching the second nitride layer. A buried oxide is grown in the substrate underneath the trench by performing thermal oxidation on the substrate. The trench is then filled by depositing an insulating layer after removing the spacer and performing a planarization process. The STI fabricating method can reduce substantially a total parasitic capacitance. Therefore, gate RC delay is reduced and the operating speed of a transistor increases. In addition, the STI fabricating method can substantially reduce junction leakage because the junction between the bottom of the source/drain and N-well or P-well is not formed. The STI fabricating method can improve isolation characteristics of P-well and N-well, and increase a circuit design margin due to the improvement of latch-up characteristic.